Amendments to the Drawings:

The attached sheet of drawing includes changes to Fig. 18. This sheet, which includes Fig. 18, replaces the original sheet including Fig. 18, correcting a minor informality noted therein.

Attachment: Replacement Sheet

REMARKS

By the above amendment, the specification has been amended to correct the informalities noted by the Examiner in the objection to the disclosure and also, submitted herewith is a replacement sheet of drawing wherein Fig. 18 has been corrected in the manner indicated by the Examiner. Accordingly, applicants submit that the objection to the disclosure and the objection to the drawing should now be overcome.

Additionally, by the present amendment, the claims have been amended to clarify the features of the present invention as being directed to a method and system for evaluating a pattern of a semiconductor device to be fabricated and that the database stores a relationship between feature indices of each three-dimensional pattern shape of a first semiconductor device to be fabricated and device properties of the fabricated first semiconductor device containing patterns each having the feature index. Furthermore, each of the independent claims of this application has been amended to recite the feature of estimating properties of another semiconductor device to be fabricated formed by the pattern to be evaluated on the basis of the quantified feature indices of three-dimensional pattern shape and information which has been stored. That is, in accordance with the present invention as illustrated in Figs. 3 and 4 of the drawings of this application, a relationship between information on a feature index of a three-dimensional pattern shape is obtained by measuring a first wafer by using a three-dimensional pattern shape evaluating means 1002, and information obtained by evaluating the device properties of the fabricated first wafer, after completion of all processing steps, by using the device property evaluating means 105, is effected, wherein the results of the evaluation is accumulated and stored in a database 401, and thereafter, the

device properties of a second wafer to be fabricated is estimated by comparing the data obtained by measuring the second wafer, using the three-dimensional pattern shape evaluating means 1002, with the data accumulated in the database 401. Applicants submit that such features are now clearly recited in the independent and dependent claims of this application, under consideration.

As to the rejection of claims 1 - 6 and 9 - 14 under 35 USC 103(a) as being unpatentable over Shishido et al (Pub. No. 2003/0015660) in view of Ponnapalli et al (US Patent No. 6,175,947) and the rejection of claims 7 - 8 and 15 - 16 under 35 USC 103(a) as being unpatentable over Shishido et al (Pub. No. 2003/0015660) in view of Ponnapalli et al (US Patent No. 6,175,947) and in further view of Solomon et al (US Patent No. 5,900,663), such rejections are traversed insofar as they are applicable to the present claims and reconsideration and withdrawal of the rejections are respectfully requested.

As to the requirements to support a rejection under 35 USC 103, reference is made to the decision of In re Fine, 5 USPQ 2d 1596 (Fed. Cir. 1988), wherein the court pointed out that the PTO has the burden under '103 to establish a prima facie case of obviousness and can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. As noted by the court, whether a particular combination might be "obvious to try" is not a legitimate test of patentability and obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching or suggestion supporting the combination. As further noted by the court, one cannot use hindsight reconstruction to pick and

choose among isolated disclosures in the prior art to deprecate the claimed invention.

In setting forth the rejection, the Examiner recognizes that Shishido et al does not disclose database storing means and device property estimating means as recited in the claims. That is, applicants submit that Shishido et al discloses a method for evaluating a pattern shape using data obtained by measuring a pattern formed with etching with a CD-SEM after storing information in a database obtained by measuring a feature index of a pattern shape using a CD-SEM, which corresponds somewhat to the three-dimensional pattern shape evaluating means 1002 in Figs. 3 and 4 of the drawings of this application. However, as recognized by the Examiner, Shishido et al does not disclose, referring to the features of claim 1, as amended, for example, a database storing means for storing the database that records therein a relationship between feature indices of each three-dimensional pattern shape of a first semiconductor device to be fabricated and device properties of the fabricated first semiconductor device containing patterns each having the feature index, and device property estimating means for estimating properties of another semiconductor device to be fabricated formed by the pattern to be evaluated on the basis of the feature indices of the three-dimensional pattern shape, which have been quantified by the feature index calculating means, and the information recorded in the database stored in the database storing means. Thus, such features, which are essentially present in each of the independent claims of this application, under consideration, as apparently recognized by the Examiner, are not disclosed or taught by Shishido et al, such that all claims under consideration patentably distinguish thereover in the sense of 35 USC 103.

The Examiner recognizing the deficiencies of Shishido et al, refers to the patent to Ponnapalli et al, contending that Ponnapalli et al discloses database storing means for storing the database that records therein a relationship between feature indices of each three-dimensional pattern shape and device properties of the circuit containing patterns each having the feature index, and device property estimating means for estimating properties of a device circuit formed by the pattern to be evaluated on the basis of the feature indices of the three-dimensional pattern shape, which have been quantified by the feature index calculating means and the information recorded in the database stored in the database storing means.

Applicants submit that the Examiner has mischaracterized the disclosure of Ponnapalli et al in relation to the claimed invention. Applicants submit that Ponnapalli et al discloses a method of calculating the parasitic capacitance of a pattern on the basis of information of a three-dimensional pattern shape obtained from design data of the pattern and for modifying a circuit pattern so as to make the parasitic capacitance smaller. However, irrespective of the contentions by the Examiner, applicants submit that Ponnapalli et al does not disclose, as recited in claim 1, for example, database storing means for storing the database that records therein a relationship between feature indices of each three-dimensional pattern shape of a first semiconductor device to be fabricated and device properties of a fabricated first semiconductor device containing patterns each having the feature index, and device property estimating means for estimating properties of another semiconductor device to be fabricated formed by the pattern to be evaluated on the basis of the feature indices of the three-dimensional pattern shape, which have been quantified by the feature index calculating means, and the information recorded in the database stored in the database storing means. That is, applicants submit that

Ponnapalli et al fails to disclose estimating the device properties after completion of all processing steps by using the information obtained by measuring the three-dimensional pattern shape as recited, the claims of this application. Accordingly, applicants submit that Ponnapalli et al also fails to disclose or teach the recited features of the independent claims of this application in the sense of 35 USC 103 and that all claims under consideration patentably distinguish over the proposed combination of Shishido et al and Ponnapalli et al in the sense of 35 USC 103. Thus, all claims under consideration should be allowable thereover.

As to the further addition of Solomon et al to the proposed combination of Shishido et al and Ponnapalli et al, applicants submit that irrespective of the Examiner's contentions concerning Solomon et al, Solomon et al also fails to overcome the deficiencies of Shishido et al and Ponnapalli et al, as pointed out above. That is, Solomon et al, like Shishido et al and Ponnapalli et al fails to disclose device property estimating means for estimating properties of another semiconductor device to be fabricated formed by the pattern to be evaluated, on the basis of the feature indices of the three-dimensional pattern shape, which have been quantified by the feature index calculating means, and the information recorded in the database stored in the database stored in the database storing means, obtained in the manner set forth. Accordingly, applicants submit that all claims also patentably distinguish over Solomon et al in the sense of 35 USC 103 and that all claims under consideration patentably distinguish over the proposed combination of Shishido et al, Ponnapalli et al and Solomon et al in the sense of 35 USC 103 and all claims should be considered allowable thereover.

In view of the above amendments and remarks, applicants submit that all claims under consideration, should now be in condition for allowance and issuance of an action of favorable nature is courteously solicited.

To the extent necessary, applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, LLP, Deposit Account No. 01-2135 (Case: 520.43079X00), and please credit any excess fees to such deposit account.

Respectfully submitted,

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